CMOS INTEGRATED CIRCUIT DEVICES AND SUBSTRATES HAVING BURIED SILICON GERMANIUM LAYERS THEREIN AND METHODS OF FORMING SAME

Abstract of the Disclosure

CMOS integrated circuit devices include an electrically insulating layer and an unstrained silicon active layer on the electrically insulating layer. An insulated gate electrode is also provided on a surface of the unstrained silicon active layer. A $Si_{1-x}Ge_x$ layer is also disposed between the electrically insulating layer and the unstrained silicon active layer. The $Si_{1-x}Ge_x$ layer forms a first junction with the unstrained silicon active layer and has a graded concentration of Ge therein that decreases monotonically in a first direction extending from a peak level towards the surface of the unstrained silicon active layer. The peak Ge concentration level is greater than $x=0.15$ and the concentration of Ge in the $Si_{1-x}Ge_x$ layer varies from the peak level to a level less than about $x=0.1$ at the first junction. The concentration of Ge at the first junction may be abrupt. More preferably, the concentration of Ge in the $Si_{1-x}Ge_x$ layer varies from the peak level where $0.2<x<0.4$ to a level where $x=0$ at the first junction. The $Si_{1-x}Ge_x$ layer also has a retrograded arsenic doping profile therein relative to the surface. This retrograded profile may result in the $Si_{1-x}Ge_x$ layer having a greater concentration of first conductivity type dopants therein relative to the concentration of first conductivity type dopants in a channel region within the unstrained silicon active layer. The total amount of dopants in the channel region and underlying $Si_{1-x}Ge_x$ layer can also be carefully controlled to achieve a desired threshold voltage.